REMARKS

This response argues specifically against the Examiner's citation of U.S. Patent No. 5,884,070 ("Panwar") under 35 U.S.C. §102(b) (Note: the Examiner cited §102(a); but we presume that the Examiner actually intended §102(b) since the current rejection refers to the printed publication of Panwar) and §103. Panwar is cited against each claim 1, 3, 8-12, 15-16 under §102 and against claims 2, 13, 14 under §103.

The remainder of the rejections in the Final Action are repeat rejections concerning claims 4, 5 and 7. Specifically, claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,371,684 to Iadonato et al. ("Iadonato") in view of U.S. Patent No. 6,598,149 to Clift ("Clift"); claims 4, 5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,826,055 to Wang et al. ("Wang") and Clift. As to these claims, we incorporate fully our arguments filed December 7, 2004 as sufficient to overcome this cited art and, as necessary, shall use these arguments in appeal.

But we ask that the Examiner reconsider the application of Panwar against claims 1-3, 8-16, at least, because Panwar does not teach or suggest the elements of these claims. Generally, the immediate application discloses register aliasing with data hazard detection logic of a processor. In an example of operation, two or more groups of registers of a stacked register file are aliased to one group of register IDs within the logic. Data hazards within registers of the multiple groups of registers are then detected by comparing register IDs; each ID aliasing to one register within each group.

This is not what Panwar discloses. Instead, Panwar discloses that "for single precision operations using aliased registers, there are at least four possible dependencies per instruction since each source register can have two possible dependencies." See Panwar col. 4, lines 11-14. Panwar does not disclose a method of reducing complexity of hazard logic through use of aliasing. In stead, Panwar discloses that "the single precision instruction, which could normally have up to four dependencies, is divided into two separate microinstructions wherein each microinstruction would have possibly only two data dependencies." See Panwar col. 6, lines 4-8. Panwar thus concerns aliasing of two single precision registers to one double precision registers, and clearly provides a very different invention for the specific case

of single precision instructions. In fact, Panwar only reduces four dependencies to two dependencies for single precision instructions.

There is thus no concept in Panwar of groups of registers utilizing common register IDs and overlapping data hazard detect logic (as for example described in independent claims 1, 8, 13, 15, 16). This aliasing within hazard detection logic enables, for example, 32 register IDs to map a large register file into 32 register sequences (claim 6) and yet with the same normal 32-row data hazard logic as before.

The Examiner refers to FIG. 1A and 1B of Panwar; but these figures clearly do not disclose the use of register IDs as claimed. FIG. 1A and 1B are discussed in the 'background art' of Panwar and specifically illustrate how two single precision registers (e.g., f5 and f4) alias to a single double precision register f4 (see Panwar, column 4, lines 9-15). According to Panwar, aliasing means two or more addresses refer to the same datum.

And Panwar does not disclose – anywhere - how data hazard detect logic is overlapping in the detection of hazards through the register IDs. Panwar can in fact utilize the background (prior art) hazard detect logic and schema shown in FIG. 1 and FIG. 2 of the present application!

Accordingly, there is no disclosure within Panwar of key features of the present claims:

- Claim 1 for example requires that "the first and second register identifiers overlap in hazard detect logic across two or more rows of the register file."
- Claim 8 requires "determining data hazards within the register file by processing one or more of the register identifiers."
- Claim 11 requires "evaluating matches between entries of the register ID file in the hazard logic without distinguishing between common aliased entries of the register file."
- Claim 15 requires "determining data hazards by matching register IDs within the data hazard logic."
- Claim 16 requires "aliasing two or more groups of registers of a stacked register file to one group of register IDs within the data hazard detection logic."

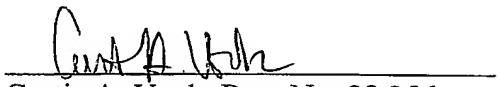
Panwar does not disclose or suggest these features (among others). Where for example does Panwar "evaluate matches between entries of the register ID file in data hazard logic"? Or, where does Panwar "evaluate matches between entries of the register ID file"? Or, where does Panwar disclose multiple groupings of registers aliased to one group of register IDs as per claims 1, 8, 16? Panwar simply does not have any such disclosure.

U.S. Patent No. 5,706,478 ("Dye") was cited with Panwar presumably because Dye discloses a 128-register register file. The Examiner then contends that a combination with Panwar with Dye renders claims 2, 3, 14 obvious. But this combination still fails to disclose the use of overlapping data hazard detect logic based on register IDs as in the present claims. Dye instead discloses a processor that "executes display list commands in processor and coprocessor mode and dynamically switches between these two modes." See Dye col. 3, lines 29-32. Dye does not disclose data hazard detection logic within the processor, nor does Dye teach or suggest aliasing of registers.

The Examiner contends that Panwar does disclose this data hazard detect logic; however we cannot find it at all within Panwar. Simply the illustration that single precision registers may be "aliased" to a double precision register is not equivalent.

We believe no additional fees are due in connection with this Response; however, if any additional fee is deemed necessary, the Examiner is authorized to charge such fee to Deposit Account No. 08-2025.

Respectfully submitted,

By: 

Curtis A. Vock, Reg. No. 38,356
LATHROP & GAGE L.C.
4845 Pearl East Circle, Suite 302
Boulder, Colorado 80301
Telephone: (720) 931-3011
Facsimile: (720) 931-3001